CLAIMS

No claims are amended, added, or canceled by this response. For the Examiner's convenience, a copy of all pending claims and a status of the claims is provided below.

1. (Previously Presented) A method of semiconductor fabrication, comprising the steps of:

forming a sidewall image transfer (SIT) loop on a substrate such that the SIT loop forms a hard mask having a width substantially equal to a critical width of a narrow section of a target shape;

protecting a pair of critical edges of the hard mask on the substrate with a first portion of a follow-on mask, wherein a width of the first portion of the follow-on mask exceeds the critical width by an amount of overlap, and a width of a wide section of the follow-on mask exceeds a width of a wide section of the target shape;

removing an exposed portion of the hard mask that is not covered by the follow-on mask; and

exposing the pair of critical edges of the hard mask by etching the follow-on mask to reduce the width of the first portion of the follow-on mask to less than the critical width.

2. (Canceled)

3. (Canceled)

4. (Previously Presented) The method of claim 1, wherein the exposing the pair of critical edges of the hard mask comprises etching the first portion of the follow-on mask from a side of the first portion of the follow-on mask.

5. (Previously Presented) The method of claim 4, further comprising removing a section of a sidewall of the wide section of the follow-on mask and then replacing a portion of the removed section of the sidewall of the wide section of the follow-on mask.

6. (Previously Presented) The method of claim 5, further comprising replacing a portion of the removed section of the sidewall of the second portion of the follow-on mask so that the second portion of the follow-on mask substantially aligns with the wide section of the target shape.

7. (Original) The method of claim 1, further comprising sizing the first portion of the follow-on mask to protect the critical edges of the hard mask when the follow-on mask is mis-registered by less than a predetermined amount.

8. (Previously Presented) A method of semiconductor fabrication, comprising the steps of:

forming a sidewall image transfer (SIT) loop on a substrate such that the SIT loop forms a hard mask, wherein a width of the hard mask substantially equals a width of a narrow section of a target shape;

forming a follow-on mask in a loop-cutter pattern on a portion of the hard mask, wherein the follow-on mask comprises a wide-image section having a width that exceeds a width of a wide section of the target shape and a narrow-image section having a width that exceeds the width of the hard mask;

removing a portion of the hard mask left exposed by the follow-on mask; and

removing at least a portion of the narrow-image section of the follow-on mask.

9. (Original) The method of claim 8, further comprising sizing the narrow-image section to cover a portion of the hard mask when the follow-on mask is mis-registered by less than a prescribed amount.

10. (Original) The method of claim 8, further comprising sizing the wide-image section of the follow-on mask to substantially align with a corresponding wide section of a final structure.

11. (Canceled)

12. (Previously Presented) The method of claim 8, further comprising reducing the width of the narrow image section of the follow on mask to an amount less than the width of the hard mask by removing at least a portion of the narrow-image section of the follow-on mask by etching the narrow-image section of the follow-on mask from at least either a side or a top of the narrow-image section of the follow-on mask.

13. (Original) The method of claim 12, further comprising forming a re-shaped follow-on mask by re-depositing material onto the wide-image section of the follow-on mask to substantially align the re-shaped follow-on mask with a corresponding portion of a final shape.

14. (Original) The method of claim 8, further comprising removing at least a portion of the narrow-image section of the follow-on mask by etching the narrow-image section of the follow-on mask from both a side and a top of the narrow-image section of the follow-on mask.

15. – 20 (Canceled)

21. (Previously Presented) A method of combining a wide-image mask and loop-cutter mask, comprising the steps of:

forming a sidewall image transfer (SIT) hard mask loop on a substrate, wherein a width of a narrow section of a target shape substantially equals a width of the hard mask loop, and a width of a wide section of the target shape exceeds the width of the hard mask loop;

forming a follow-on mask over a portion of the hard mask loop, wherein the follow-on mask includes a first section corresponding to the wide section of the target shape and a second section overlapping the narrow section of the target shape, and a width of the second section of the follow-on mask exceeds the width of the narrow section of the target shape;

removing regions of the hard mask loop uncovered by the follow on mask;

etching the second section of the follow-on mask to expose underlying edges of the hard mask loop;

etching the first section of the follow-on mask to reduce its length and width to produce an image pad that substantially conforms to the wide section of the target shape; and

etching the substrate uncovered by the remaining hard mask loop and image pad.

22. (Previously Presented) The method of claim 21, wherein the etching the second section of the follow-on mask to expose underlying edges of the hard mask loop comprises completely removing the second section of the follow-on mask from the narrow section of the hard mask loop.

23. (Previously Presented) The method of claim 22, wherein the SIT hard mask loop is formed using a non-photolithographic imaging technique.

24. (Previously Presented) The method of claim 23, wherein the SIT hard mask loop is a few tens of nanometers wide.

25. (Previously Presented) The method of claim 1, wherein the SIT loop is formed using a non-photolithographic imaging technique.

26. (Previously Presented) The method of claim 25, wherein the SIT loop is a few tens of nanometers wide.

27. (Previously Presented) The method of claim 1, further comprising:

reducing a length and the width of the wide section of the follow-on mask to form a core pad that is smaller than the wide section of the target shape; and

re-growing the follow-on mask along edges of the core pad to form an image pad that substantially conforms to the wide section of the target shape.

28. (Previously Presented) The method of claim 8, further comprising:

reducing a length and the width of the wide-image section of the follow-on mask to form a core pad that is smaller than the wide section of the target shape; and

re-growing the follow-on mask along edges of the core pad to form an image pad that substantially conforms to the wide section of the target shape.